Remarks/Arguments

Examiner Arora is thanked for the thorough examination and search of the subject patent application.

Claims 1, 4, 7, 9-12, 15, 17-19, 21, 22, 25, 27, 29, 30, 91, 96-99, 101-103 and 108-139 are pending; Claims 1, 9-12, 15, 19, 21, 22, 25, 27, 91, 97 and 102 have been currently amended; Claims 108-114 and 116-139 have been newly added; Claim 30 has been withdrawn; Claims 4 and 29 have been withdrawn and currently amended; Claim 115 has been withdrawn and newly added; Claims 2, 3, 5, 6, 8, 13, 14, 16, 20, 23, 24, 26, 28, 31-90, 92-95, 100 and 104-107 have been canceled. No new matter is believed to have been added.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 1, 4, 7, 91, 96, 97, 113-117 and 123-128

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As currently amended, independent Claim 1 is recited below:

1. An integrated circuit chip comprising:
a semiconductor substrate;
a transistor in and on said semiconductor substrate;
multiple metal and dielectric layers over said semiconductor substrate;
a first contact pad over said semiconductor substrate;
a second contact pad over said semiconductor substrate;
a passivation layer over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening;
a power metal structure over said passivation layer and on said first contact point, wherein said power metal structure is connected to said first contact point through said first opening, wherein said power metal structure comprises a copper layer, and wherein said power metal structure has a first region used to be wirebonded thereto for connection made to a next level of packaging;
a ground metal structure over said passivation layer and on said second contact point, wherein said ground metal structure is connected to said second contact point through said second opening, wherein said ground metal structure comprises a copper layer, and wherein said ground metal structure has a second region used to be wirebonded thereto for connection made to said next level of packaging;
a capacitor over said passivation layer and directly over said first contact point;
a first solder contact directly over said first contact point and between said capacitor and said power metal structure, wherein said first solder contact connects said capacitor to said power metal structure; and
a second solder contact between said capacitor and said ground metal structure, wherein said second solder contact connects said capacitor to said ground metal structure.

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Reconsiderations of Claims 1, 7 and 91 rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al. (U.S. Pat. No. 5,629,240) in view of Feustel et al. (U.S. Pub. No. 2002/0008967), of Claim 96 rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al. in view of Efland et al. (U.S. Pat. No. 6,020,640), and of

Claim 97 rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al. in view of Greer (U.S. Pat. No. 6,451,681) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip currently claimed in amended Claim 1 patentably distinguishes over the citation by Malladi et al. (U.S. Pat. No. 5,629,240) in view of Feustel et al. (U.S. Pub. No. 2002/0008967).

The Examiner considers that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malladi so that the said power metal structure and the said ground metal structure each comprise a copper layer." ~ *See lines 3-6 on page 4, in the last Office Action mailed Oct. 17, 2008* ~

Applicant respectfully traverses the Examiner's opinion because Feustel et al.'s metal layer 32 is believed to be non-analogous to Malladi et al.'s pads 70 and 72. Malladi et al.'s metal layer 66, 68, 70 and 72 are formed in openings in a passivation layer 32 comprising a nitride and on a top surface of the passivation layer 32. ~ *See Fig. 2B and col. 1, lines 63-65, in U.S. Pat. No. 5,629,240* ~ However, Feustel et al.'s metal layer 32 is formed on a ceramic layer 31, but is not formed on a passivation layer comprising a nitride. ~ *See para. [0020], in U.S. Pub. No. 2002/0008967* ~ Therefore, Feustel et al.'s metal layer 32 is believed not to be applied to Malladi et al.'s metal layer 66, 68, 70 and 72 because Malladi et al.'s metal layer 66, 68, 70 and 72 and Feustel et al.'s metal layer 32 are formed on a layer with different materials.

Furthermore, Malladi et al. teach that bond wires 42 and 44 can connect the pads 70 and 72 to peripheral Vss and Vdd bonding pads and power rails on IC 12, but is not for connection made to a next level of packaging. ~ *See Fig. 2B and col. 2, lines 24-26, in U.S. Pat. No. 5,629,240* ~ Therefore, the claimed subject matter that a power or ground metal structures connected to a capacitor have regions used to be wirebonded thereto for connection made to a next level of packaging, as currently claimed in Claim 1 is believed not to be anticipated by Malladi et al.'s teaching.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 1 is respectfully requested.

Applicants respectfully submit independent Claim 1 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 4, 7, 91, 96, 97, 113-117 and 123-128 patentably define over the prior art as well.

Response to Claims 9-12, 98, 99 and 118-122

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As currently amended, independent Claim 9 is recited below:

9. An integrated circuit chip comprising:
a semiconductor substrate;

a transistor in and on said semiconductor substrate;
multiple metal and dielectric layers over said semiconductor substrate;
a first contact pad over said semiconductor substrate;
a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, and wherein said passivation layer comprises a nitride;
a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein the position of said second contact pad from a top perspective view is different from that of said first contact point, and wherein said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer;
a capacitor over said passivation layer and over said second contact pad;
a solder contact between said capacitor and said second contact pad, wherein said solder contact connects said capacitor to said second contact pad; and
electroplated copper between said solder contact and said second contact pad.

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Reconsiderations of Claims 9-12, 98 and 99 rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al. (U.S. Pat. No. 5,629,240) in view of Master (U.S. Pub. No. 2003/0037959) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip currently claimed in amended Claim 9 patentably distinguishes over the citation by Malladi et al. (U.S. Pat. No. 5,629,240) in view of Master (U.S. Pub. No. 2003/0037959).

The Examiner considers that "In this case, Master teaches a chip with contact pads to which components may be attached by solder connection, wherein there is an additional metal layer between said solder connection and said second contact pad (page

2, paragraph 0027), which is similar to the teachings of connecting a capacitor to a chip of Malladi." ~ *See lines 2-6 on page 16, in the last Office Action mailed Oct. 17, 2008* ~

Applicant respectfully traverse the Examiner's opinion because even though both Master's flip-chip process and Malladi et al.'s capacitor mounting process of connecting a capacitor to a chip can be performed using a solder, Master's flip-chip process is dramatically not similar to Malladi et al.'s capacitor mounting process. Master's flip-chip process relates to how a chip at an upper side is mounted on a circuit substrate, such as printed circuit board (PCB). Malladi et al.'s capacitor mounting process relates to how an IC 12 at a lower side has a capacitor 74 mounted thereon. Master's flip-chip process is believed to be non-analogous to Malladi et al.'s capacitor mounting process because the relative position of Master's chip, during the flip-chip process, at an upper side is different from that of Malladi et al.'s IC 12, during the capacitor mounting process, at a lower side.

Furthermore, both Malladi et al. and Master fail to teach, hint or suggest the claimed subject that electroplated copper is between a solder contact and a contact pad having a capacitor provided thereover, as currently claimed in Claim 9. ~ *See lines 17-19 on page 12, in the last Office Action mailed Oct. 17, 2008* ~

The Examiner considers that "the thickness of the gold layer is considered to involve routine optimization, which has been held to be within the level of ordinary skill in the art."

Applicant respectfully traverses the Examiner opinion. If the Examiner considers the claimed subject matter that a contact pad having electroplated copper and a solder contact provided thereover can comprise a gold layer with a thickness greater than 1 micrometer, as currently claimed in Claim 9 involves routine optimization and has been held to be within the level of ordinary skill in the art, showing an evidence of this is respectfully requested.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 9 is respectfully requested.

Applicants respectfully submit independent Claim 1 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 10-12, 98, 99 and 118-122 patentably define over the prior art as well.

Response to Claims 15, 17-19, 21, 22, 25, 27, 29, 30, 101-103 and 108-112

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As currently amended, independent Claim 15 is recited below:

15. An integrated circuit chip comprising:
a semiconductor substrate;
a transistor in and on said semiconductor substrate;
multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride, and wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening;

a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening;

a third contact pad over said semiconductor substrate, wherein said third contact pad is connected to said first contact point through said first opening and connected to said second contact pad, wherein the position of said third contact pad from a top perspective view is different from that of said first contact point, and wherein said third contact pad has a region used to be wirebonded thereto for connection made to a next level of packaging;

a first polymer layer over said passivation layer, wherein a second opening in said first polymer layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening;

a capacitor over said first polymer layer and over said second contact point; and

a solder contact between said second contact point and said capacitor, wherein said solder contact connects said capacitor to said second contact point.

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Reconsiderations of Claims 15, 17-19, 21, 22, 25, 27 and 101-103 rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al. (U.S. Pat. No. 5,629,240) in view of Greer (U.S. Pat. No. 6,451,681) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip currently claimed in amended Claim 15 patentably distinguishes over the citation by Malladi et al. (U.S. Pat. No. 5,629,240) in view of Greer (U.S. Pat. No. 6,451,681).

Greer teaches that both an opening in a passivation layer 300 and an opening in a polymer layer 302 are over a same contact point of a contact pad 312. ~ *See Figs. 3 and 4 in U.S. Pat. No. 6,451,681* ~ However, Greer fails to teach, hint or suggest the claimed

subject matter that a second contact point at a bottom of a second opening in a polymer layer can be connected to a first contact point at a bottom of a first opening in a passivation layer through the first opening, as currently claimed in Claim 15. Therefore, the claimed subject matter that a second contact point at a bottom of a second opening in a polymer layer can be connected to a first contact point at a bottom of a first opening in a passivation layer through the first opening, as currently claimed in Claim 15 is believed to unobvious over Malladi et al.'s teaching in view of Greer's teaching.

The Examiner considers that "The ordinary artisan would be motivated to modify Malladi at least for the purpose of providing an additional protection layer over the metallization but providing openings in the polymer layer (just like openings in passivation layer) as required to form interconnections." ~ *See line 19 of page 6 through line 2 of page 7, in the last Office Action mailed Oct. 17, 2008* ~

Applicant respectfully traverses the Examiner's opinion because Greer's polymer layer 302 is believed not to be applied to Malladi et al.'s device. Greer's polymer layer 302 is used on a passivation layer for a flip-chip process having a solder bump 310 formed thereover and for a wirebonding process having a wirebond 404 bonded thereon. ~ *See Figs. 3 and 4, and col. 4, line 59 through col. 5, line 42, in U.S. Pat. No. 6,451,681* ~ However, Greer fails to teach, hint or suggest that Greer's polymer layer 302 can be used on a passivation layer comprising a nitride for a capacitor-mounting process. A flip-chip process relates to how a chip at an upper side is mounted on a circuit substrate, such as printed circuit board (PCB). Malladi et al.'s capacitor mounting process relates to how an

IC 12 at a lower side has a capacitor 74 mounted thereon. Therefore, the flip-chip process is believed to be non-analogous to Malladi et al.'s capacitor mounting process because the relative position of the chip, during the flip-chip process, at an upper side is different from that of Malladi et al.'s IC 12, during the capacitor mounting process, at a lower side. Greer's polymer layer 302 for a flip-chip process is believed not to be readily applied to Malladi et al.'s device because the flip-chip process is believed to be non-analogous to Malladi et al.'s capacitor mounting process.

Furthermore, Malladi et al. teach that bond wires 42 and 44 can connect the pads 70 and 72 to peripheral Vss and Vdd bonding pads and power rails on IC 12, but is not for connection made to a next level of packaging. ~ *See Fig. 2B and col. 2, lines 24-26, in U.S. Pat. No. 5,629,240* ~ Therefore, the claimed subject matter that a third contact pad connected to a second contact pad having a capacitor provided thereover has a region used to be wirebonded thereto for connection made to a next level of packaging, as currently claimed in Claim 15 is believed not to be anticipated by Malladi et al.'s teaching.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 15 is respectfully requested.

Applicants respectfully submit independent Claim 15 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent

Claims 17-19, 21, 22, 25, 27, 29, 30, 101-103 and 108-112 patentably define over the prior art as well.

For at least the same reasons, new claims 108 to 139 are believed to patentably define over the prior art as well.

Conclusion

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Arora not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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